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**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

Claim 1 (previously presented): An electronic substrate to mount a plurality of semiconductor chips thereon, the substrate comprising:

a first conductive member, which is electrically connected to one of the semiconductor chips;

a second conductive member, which is electrically connected to another one of the semiconductor chips; and

an insulating layer for electrically isolating the second conductive member from the first conductive member; wherein

the first conductive member is a conductive base that supports the insulating layer, the semiconductor chips and the second conductive member thereon;

a connector extends through the insulating layer; and

a first power supply electrode is provided on the insulating layer and is electrically connected to the conductive base by said connector.

Claim 2 (original): The electronic substrate of claim 1, wherein the insulating layer is provided on the conductive base, a patterned conductive film is defined on the insulating layer, and a portion of the patterned conductive film functions as the second conductive member.

Claim 3 (original): The electronic substrate of claim 2, further comprising:

a first power supply electrode, which is electrically connected to the conductive base; and

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a second power supply electrode, which is electrically connected to the second conductive member; wherein

while the semiconductor chips are ON, the first and second power supply electrodes are connected to an external power supply.

Claim 4 (original): The electronic substrate of claim 3, wherein the first power supply electrode is provided on the insulating layer and is electrically connected to the conductive base by way of an opening which is arranged so as to extend through the insulating layer.

Claim 5 (original): The electronic substrate of claim 4, wherein the conductive base is provided with a plurality of recesses, a first conductive pin is inserted into one of the recesses of the conductive base so as to electrically connect the conductive base to the first power supply electrode, and a second conductive pin is inserted into another one of the recesses of the conductive base so as to electrically connect the conductive base to another portion of the patterned conductive film.

Claim 6 (original): The electronic substrate of claim 5, wherein the direction of a current flowing through an inside portion of the conductive base between the first and second conductive pins is substantially opposite to that of a current flowing through an inside portion of the second conductive member, the inside portion of the second conductive member overlapping with that of the conductive base.

Claim 7 (original): The electronic substrate of claim 1, wherein the conductive base is a metal plate with a thickness of at least about 1 mm, and the conductive base has a flat back surface that is capable of making a thermal contact with a heat sink.

Claim 8 (original): The electronic substrate of claim 3, wherein the second conductive member and the first and second power supply electrodes are defined by patterned metal foil.

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Claim 9 (original): The electronic substrate of claim 4, wherein the second conductive member and the first and second power supply electrodes are defined by patterned metal foil.

Claim 10 (original): The electronic substrate of claim 3, wherein while the semiconductor chips are ON, a current flowing between the first and second power supply electrodes has a maximum value of at least about 50 amperes.

Claim 11 (original): The electronic substrate of claim 4, wherein while the semiconductor chips are ON, a current flowing between the first and second power supply electrodes has a maximum value of at least about 50 amperes.

Claim 12 (original): The electronic substrate of claim 1, wherein the insulating layer is made of an epoxy resin with a thickness of about 0.2 mm or less.

Claim 13 (previously presented): A power module comprising:  
a plurality of power semiconductor chips;  
a first conductive member, which is electrically connected to one of the power semiconductor chips;  
a second conductive member, which is electrically connected to another one of the power semiconductor chips; and  
an insulating layer for electrically isolating the second conductive member from the first conductive member; wherein  
the first conductive member is a conductive base that supports the insulating layer, the power semiconductor chips and the second conductive member thereon;  
a connector extends through the insulating layer; and  
a first power supply electrode is provided on the insulating layer and is electrically connected to the conductive base by said connector.

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Claims 14-18 (canceled).

Claim 19 (currently amended): An electronic substrate to mount a plurality of semiconductor chips thereon, the substrate comprising:

a first conductive member, which is electrically connected to one of the semiconductor chips;

a second conductive member, which is electrically connected to another one of the semiconductor chips;

an insulating layer for electrically isolating the second conductive member from the first conductive member; and

a conductive base that supports the first and second conductive members, the insulating layer and the semiconductor chips thereon; wherein

the second conductive member is a conductive plate, which is large enough to mount at least one of the semiconductor chips thereon;

the conductive plate is supported on the conductive base so as to cover at least a portion of the first conductive member; and

The electronic substrate of claim 18, wherein the direction of a current flowing through the conductive plate is substantially opposite to that of a current flowing through the portion of the first conductive member under the conductive plate.

Claim 20 (canceled).

Claim 21 (original): The electronic substrate of claim 19, wherein the insulating layer includes at least one of a silicone sheet, a polyimide film, an epoxy resin and an air layer.